

## **AMENDMENTS TO THE SPECIFICATION:**

Please replace the paragraph beginning at page 2, line 8, with the following rewritten paragraph:

1       The operation of the Pixel Block is as follows: Node IN is connected to  
2 switch RES, the cathode of photodiode ~~photofide~~ PD, and the gate of NMOS  
3 transistor N1. Initially switch RES is closed and the voltage on node IN is VRES.  
4 Then switch RES is opened. There will be a finite charge on node IN dependent  
5 on the voltage VRES, the capacitance of photodiode PD, and the gate  
6 capacitance of NMOS transistor N1. The photodiode current causes the charge  
7 on node IN to be discharged and the voltage on node IN decreases. Generally  
8 imagers have a fixed integration time or period. The voltage on node IN at the  
9 end of the integration period is referred to herein as VPD.